ECE 515/514
Fall 2013

INTRODUCTION TO VLSI SYSTEMS

Tue+Thu: 9:30-10.45, Lutz 306

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The purpose of this course is to teach the students basic methodology of structured digital VLSI circuit design in CMOS technology and develop VLSI design experience.

Prerequisites: ECE/CECS 210, co-requisite ECE/CECS 510 (or equivalent courses) (ECE 515, CECS 525 or consent of the instructor may be substituted as a co-requisite).

Class website: http://ci.louisville.edu/zurada/courses/ece515/ (for orientation only), only BB contains current information

TOPIC	Wks	COMMENTS
0.Introduction to VLSI design and CAD tools	1	VLSI Lab, Classroom, WSS221
1. Stick diagrams/gate arrays, MOS transistors, NMOS/CMOS inverters, transfer characteristics, noise margins, optimisation of VTC, timing considerations, NANDs and NORs.	3	Project 1 starts about here
2. Fabrication and Design Rules: photolithography process, VLSI MOS transistor fabrication scheme, lambda design rules, layout design project.	0.5	
3.Electrical parameters and scaling effects	0.5	Project 2 starts about here
4.Combinatorial VLSI Logic: logic realizations, NOR synthesis, compound gates, structured gate arrays, PLAs, pass transistor arrays, transmission gates.	3	Chip project initiated and approved
5.Register Arrays and Stack Design: clock control, static and dynamic memory cells, flip-flops, registers, LIFO arrays.	1.5	Project 3 starts about here
6.Finite State Machines: fundamentals, PLA-based implementation	1	Final chip design discussion
7.Design of VLSI Functional Blocks and Subsystems: counters, adders, ROM, and RAM cells, ALUs, etc.	2.5	Project 4 about here Final chip work
8.Overview of Semi-Custom Techniques.	0.5	Lab work ready, Rept. due
9.Tests	1.5	3 tests every 4-5 weeks each

This course involves a comprehensive VLSI circuit computer-aided layout design and simulation using L-edit/Tanner tools.

Text EE 515: Ayres, Digital Integrated Circuits Analysis and Design, 2nd edition, CRC Press ©2010, ISBN 978-1-4200-6987-7

Text EE 514: A.Abdullin, J.Chorowski, J.M. Zurada, Introduction to VLSI Systems Laboratory, ECE Dept., U of L, C 2011

Grading EE 515 (3CR): 66% Three quizzes, 22% Homework, 12% Projects
EE 514 (1CR): 100% Projects

The course may be taken as an ECE Elective, ECE Design Elective or M.S.E.E. course.
Graduate (600-level) Requirements include submitting the Final Project Report which, in addition to discussion of design and verification, also contains one of the following: (i) comparison of selected design with other design found in the technical literature, and (ii) evaluation of speed and efficiency as supported by simulation or analysis.

Course Learning Outcomes:

1. Know how to analyze loaded MOSFETs v-i characteristics for various geometries of drivers
2. Determine VTC curves of inverters with resistive, NMOS and PMOS loads
3. Be able to use load line techniques to graph VTCs
4. Determine inversion voltage and noise margins for inverters and simple NOR and NAND gates
5. Analyze basic transients, switching curves, and know how to handle charge-sharing effect
6. Design inverters geometries with various trade-offs such as area, power, noise resistance, speed, DC performance
7. Know how to model resistive and capacitive performance of interconnections and MOSFETs
8. Use modern tools for DC and transient analysis of logic switching circuits, including modeling drivers, loads using SPICE in various analysis modes
9. Be able to extract electrical parameters from layout using software extractors
10. Design combinational logic blocks with standard gates or PLAs and simulate them for logic and timing
11. Master electrical and layout design of sequential circuitry, including memories and finite state machines
12. Be able to fit a chip to be designed into a realistic, limited-size frame of the “tiny chip”, use I/O pads
13. Design a functional, testable VLSI circuitry and simulate it electrically and logically
14. Present a lab report and master presentation skills

Grade boundaries will normally be as shown in the table below

Term Total (%)	Grade
96-100	A+
93-95.99	A
90-92.99	A-
86-89.99	B+
83-85.99	B
80-82.99	B-
76-79.99	C+
73-75.99	C
70-72.99	C-
66-69.99	D+
63-65.99	D
60-62.99	D-
< 59.99	F

SAMPLES of WORK for ASSESSMENT: Copies of selected papers will be made and kept in departmental files for the purpose of accreditation-related assessment.